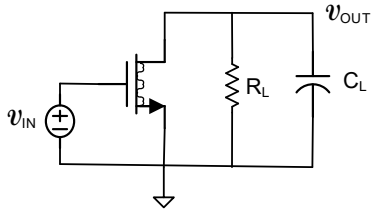
EE 330
Homework 13
Fall 2025
Due 1:00 p.m. Wednesday Nov 19 at Noon (no late submissions accepted this week)

If parameters of semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=250\mu A/V^2$, $\mu_p C_{OX}=\mu_n C_{OX}/3$,$V_{TNO}=0.4V$, $V_{TPO}= - 0.4V$, $C_{OX}=4fF/\mu^2$, $\lambda = 0$. Correspondingly, assume all npn BJT transistors have model parameters $J_S= 10^{-14}A/\mu^2$ and $\beta=100$ and all pnp BJT transistors have model parameters $J_S= 10^{-14}A/\mu^2$ and $\beta = 25$. If the emitter area of a transistor is not given, assume it is $100\mu^2$. Parasitic capacitance parameters for a sample 0.5u CMOS process appear in the Appendix.

Problem 1

The small-signal equivalent circuit of the standard common-source amplifier biased to operate in the saturation region is shown below where a ***small*** capacitor, C_L, has been placed on the amplifier output.

Express the small-signal gain of the amplifier, $A_V(s)=\dfrac{v_{OUT}(s)}{v_{IN}(s)}$, in terms of the small-signal model parameters.



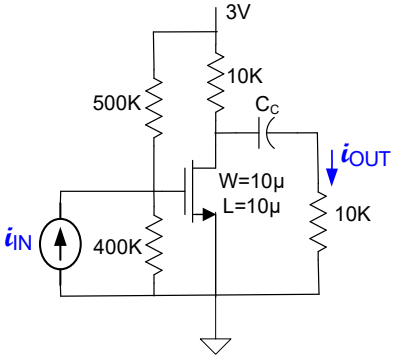
Problem 2

Consider the following amplifier where the input is a small-signal current source i_{IN}. Assume the coupling capacitor C_C is very large. Assume the transistor is in a process with $u_nC_{OX}=250uA/V^2$, $C_{OX}=4fF/u^2$, $V_{THn}=0.4V$, and $\lambda=0$. Assume all parasitic capacitances in the transistor are negligible in this circuit except for C_{GS}.

a) Draw the small-signal equivalent circuit

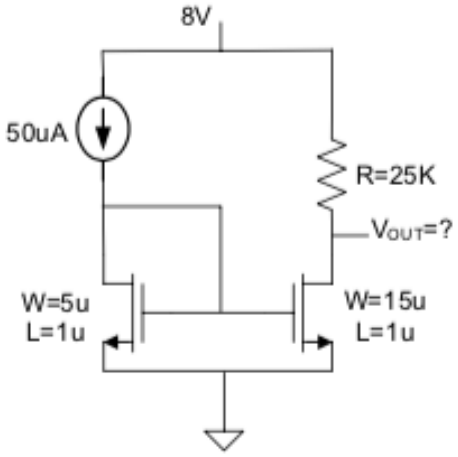
b) Determine the dc small-signal current gain $A_I=\dfrac{i_{OUT}}{i_{IN}}$

c) Determine the frequency where the magnitude of the current gain drops to one.



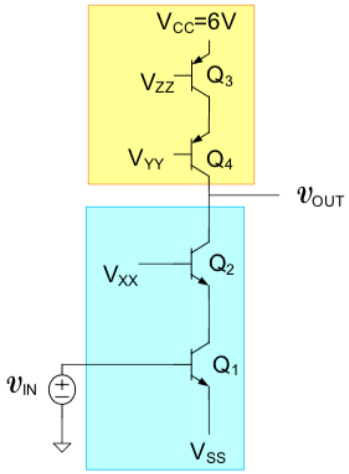
Problem 3

Find V_{OUT} for the circuit below.



Problem 4

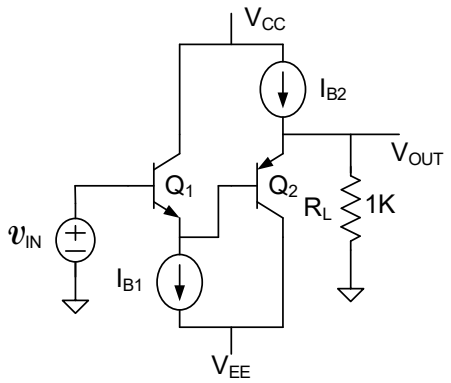
Assume the biasing voltages have been selected so that the quiescent output voltage is $2V$ and that all transisotrs are operating in the forward active region. Determine the small-signal voltage gain if $A_{E1} = A_{E2} = 40\mu^2$ and $A_{E3} = A_{E4} = 60\mu^2$. Assume the transistors all have parameters $\beta = 100$ and V_{AF}= $100V$.



Problem 5

Assume $A_{E1}=A_{E2}=5\mu^2$, $I_{B1}=I_{B2}=1mA$ and $\beta_1=\beta_2=100$. The supply voltages are +5V and -5V.

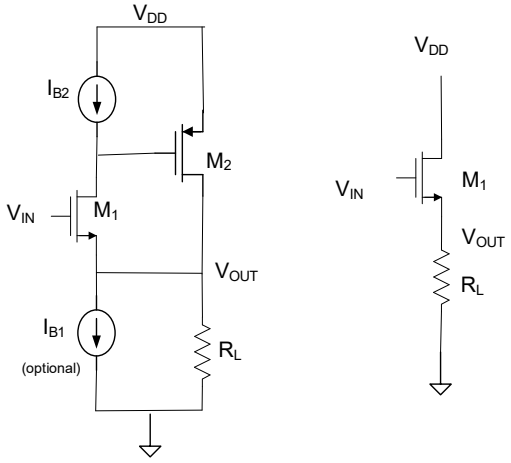
a) Determine the small signal voltage gain.
b) Determine the quiescent output voltage
c) Determine the small-signal input impedance
d) Determine the maximum output swing.



Problem 6

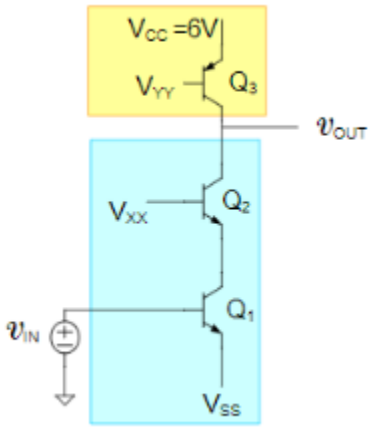
Consider the two amplifier circuit shown below where $V_{DD}=5V$, $I_{B1}=5\mu A$, $I_{B2}=10\mu A$, and $R_L=5K$. Assume the transistors are identically sized with W=10µ and L=2µ.

a) Give the small-signal voltage gain of the two amplifiers in terms of the small-signal model parameters
b) Numerically determine the small-signal voltage gain for the two amplifiers if $V_{INQ}=1V$.
c) Determine the quiescent output voltage and the difference between the quiescent output voltages of the two amplifiers if $V_{INQ}=1V$.
d) Repeat part c) if $V_{INQ}=4V$.



Problem 7

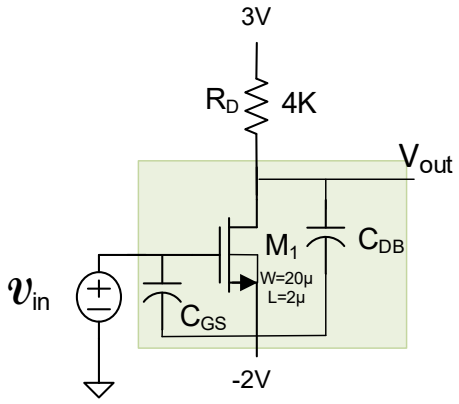
Assume the quiescent output is 2V and all transistors are in the forward active region of operation. Find the small signal voltage gain if $A_{E1}=A_{E2}=55\mu^2$ and $A_{E3}=75\mu^2$. Assume the transistors all have parameters $\beta = 100$ and $V_{AF}= 100V$.

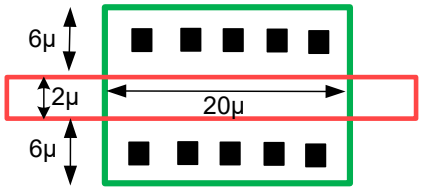


Problem 8

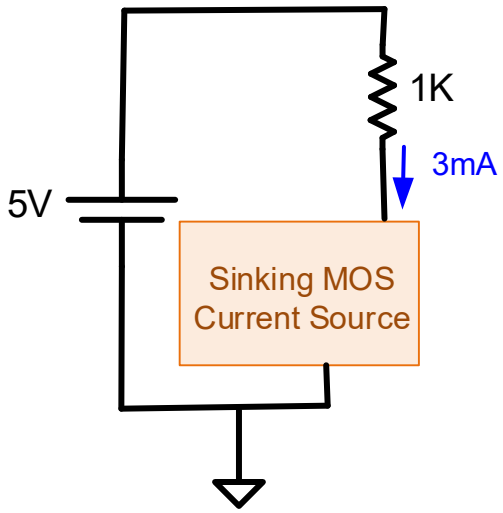
Consider the following amplifier. Assume the dominant parasitic capacitances in the transistor are C_{GS} and C_{DB}. They are depicted in the green shaded region that comprises the transistor M_1. The layout of the transistor, not to scale, is also shown below.

a) Draw the small-signal equivalent circuit that can be used to determine the high-frequency response
b) Obtain an expression for the small-signal voltage gain in terms of the small-signal model parameters
c) Determine the 3dB bandwidth (in Hz) for this amplifier.





Problem 9 Design a sinking current source that can sink a current of 3mA from a 1K resistor with one terminal connected to a 5V dc voltage source. You have available for this design any number of MOS transistor, the 5V source, and the 1K resistor.



Appendix: Parasitic Capacitances in a sample 0.5u CMOS Process

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	942	1163	106	34	14	9	6	5	3		123		125	aF/um^2
Area (N+active)			8484	55	20	13	11	9	8					aF/um^2
Area (P+active)			8232											aF/um^2
Area (poly)				66	17	10	7	5	4					aF/um^2
Area (metal1)					37	14	9	6	5					aF/um^2
Area (metal2)						35	14	9	6					aF/um^2
Area (metal3)							37	14	9					aF/um^2
Area (metal4)								36	14					aF/um^2
Area (metal5)									34			984		aF/um^2
Area (r well)	920													aF/um^2
Area (d well)										582				aF/um^2
Area (no well)	137													aF/um^2
Fringe (substrate)	212	235		41	35	29	21	14						aF/um
Fringe (poly)				70	39	29	23	20	17					aF/um
Fringe (metal1)					52	34		22	19					aF/um
Fringe (metal2)						48	35	27	22					aF/um
Fringe (metal3)							53	34	27					aF/um
Fringe (metal4)								58	35					aF/um
Fringe (metal5)									55					aF/um
Overlap (N+active)			895											aF/um
Overlap (P+active)			737											aF/um